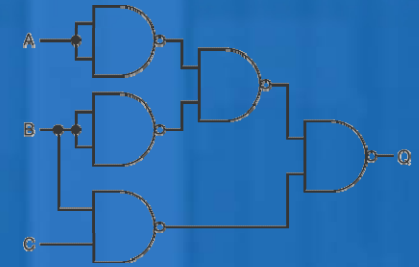


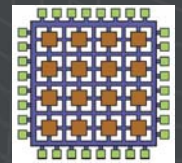
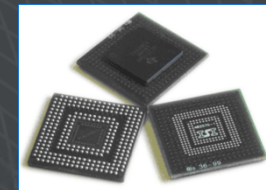
estimate



estimate • analyze • plan • control

Estimation of FPGA development Effort

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January 20, 2010



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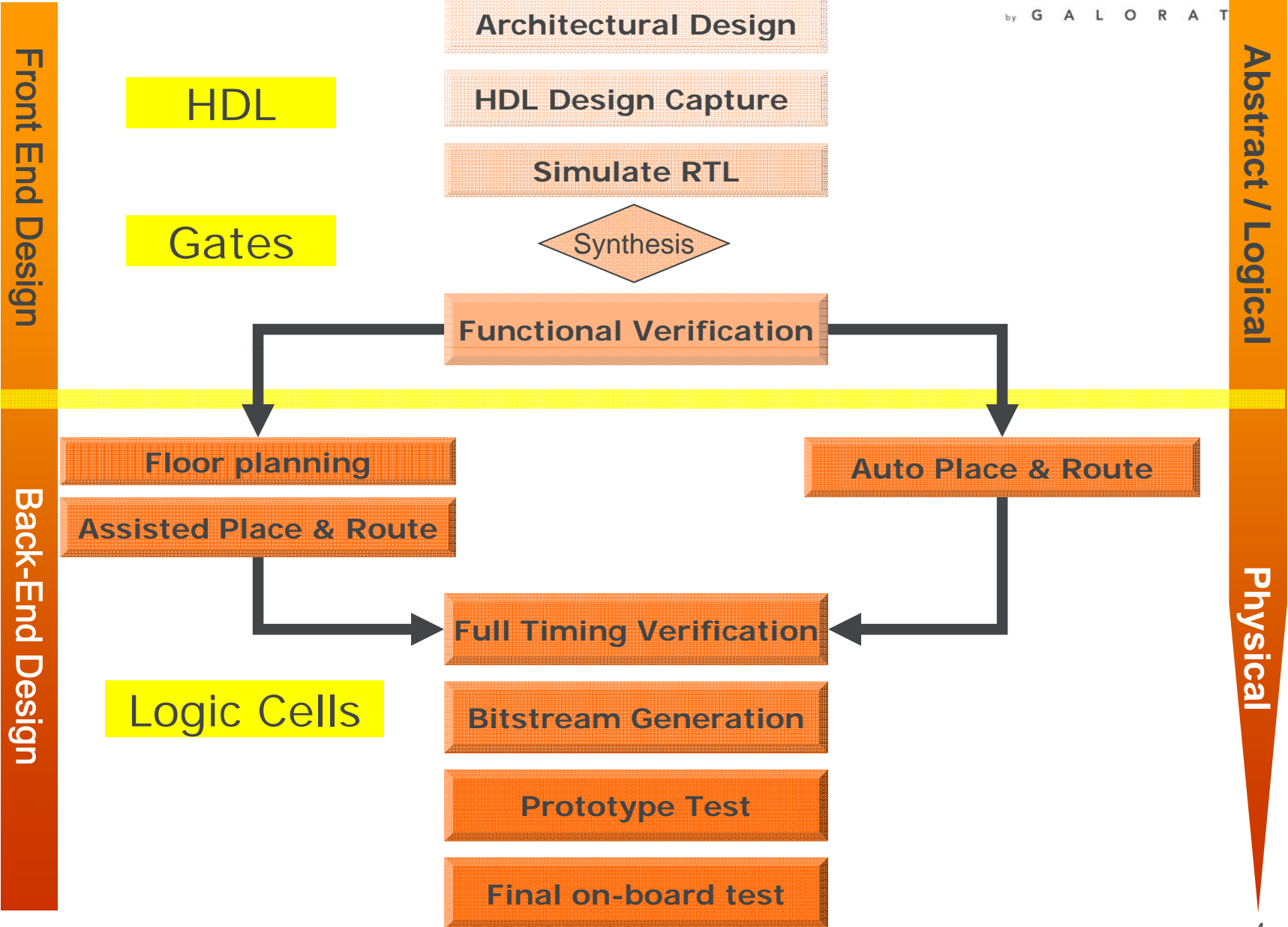
A few points

- There are numerous FPGA offerings and they are finding their way into all types of board designs.
- The FPGA development efforts starts in the high level logical world but must end down in the physical one.
- As others have mentioned, we also treat HDL effort differently from SW.
- If a design requires performance, it may gravitate to an FPGA solution, typically this option will outperform SW running on a processor (depends on application).
- There are key differences between HW and SW that must be considered during cost estimation efforts.

A few points (continue)

- In order to estimate an FPGA effort, we will briefly look at a development flow in order to examine some key cost categories.
- We'll look at some key inputs commonly used in estimating FPGA HW. We can compare these to SW approach.

FPGA COST BLOCKS



Some inputs to consider



- Environment (Ground, Space, Commercial, etc)
- Sizing parameters (SLOC, gates, Logic Cells, etc)
- Legacy Benefit (IP logic – akin to COTS SW, etc)
- Technology being used (SOC, 65nm, rad hard, etc)
- Standard being applied (DO 254?)
- Efficiency of team (People, Experience, etc)
- Efficiency of environment (location, process, stability, etc)
- Setup of process (type 1, trusted, prototyping path)
- Rigor of Verification
- Chip Utilization %

Some inputs to consider (continued)



- Performance:
 - Clock Speed
 - Complex Clocking Schemes
 - Aggressive Power Management
 - Use of complex cores

Sizing Parameters – Physical Side



Question: What can be used to differentiate a large, medium or small design?

- Sizing parameters:
 - Active Logic Cells (Xilinx)
 - Active Logic Elements (Altera)
 - System Gates
- Secondary sizing parameters:
 - Multipliers, DSP blocks
 - Transceivers
 - Registers

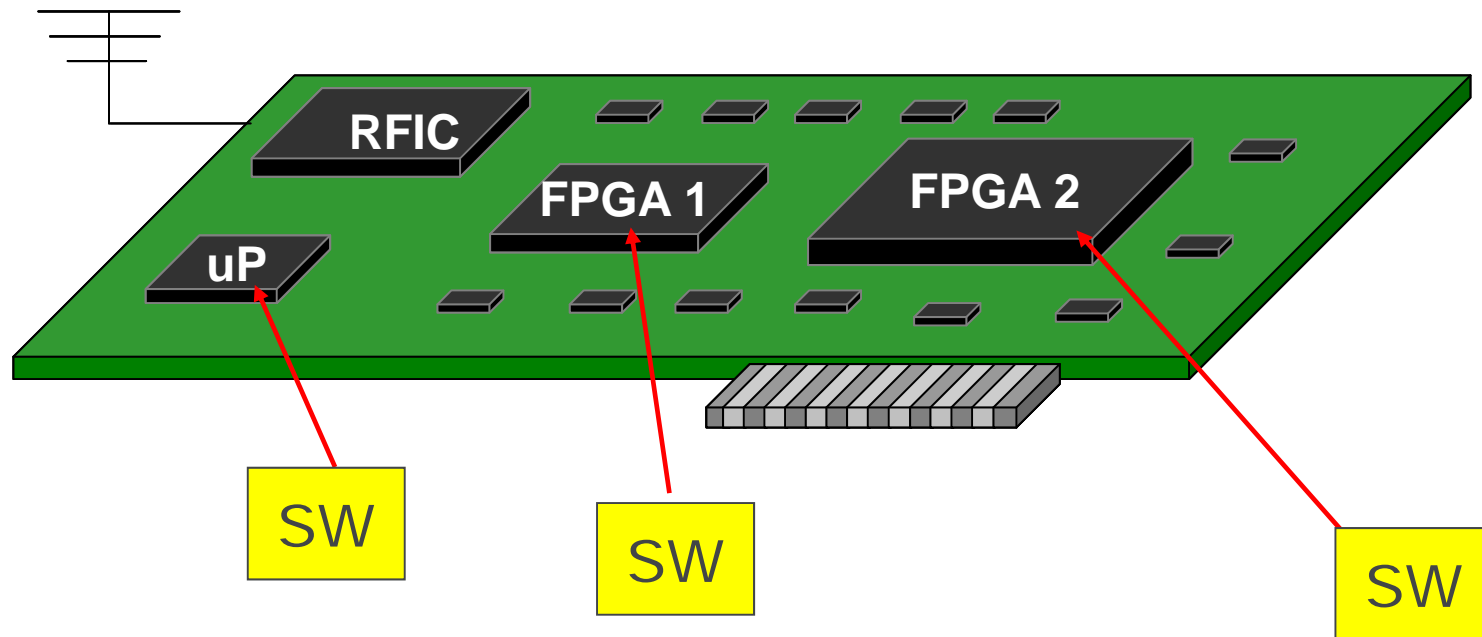
Sizing Parameters – Logical Side



- HDL lines of code ?
- Some still use this method.
- Informal survey determined that most did not like this method due to issues that tend to arise late in the design cycle (physical world) which cannot be reflected in lines of code.
- The same code can be synthesized in many ways depending to technology to be used. Some paths may lead to very challenging closures (effort/\$\$\$)

Top level Design Issues

- Allocation of functionality HW vs SW
- Integration of HW/SW process
- Multiple FPGA dies (many multiple SW)
- Timing issues
- Signal Integrity
- We assign a top level complexity to capture all Efforts below.



Conclusion



- FPGAs are found in many applications.
- The technologies have grown incredibly large and continue to add more features. One key feature is the ability to incorporate SW processors within the die itself (hard/soft cores).
- HW/SW codesign continue to present challenges to many organizations, although many EDA vendors have solutions to address this issue.
- Each organization needs to determine what technical/non-technical inputs need to be used to generate credible estimates.
- Estimate by analogy is difficult with these chips since so many things tend to change from design to design.