Estimating Space ASICs Using SEER-IC/H

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Today's Topics

- Why Estimate ASICs
- ASIC Basics
- Our Estimating Challenge
- Summary

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Why Estimate ASICs?

- ASIC devices are found in many of today's advanced electronics and high performance military designs
- There are various types of ASIC technologies each with advantages specific to the application
- Standard cell ASICs provide critical high performance specialized functionality typically not offered by other types of micro-electronics technologies (FPGAs, Structured Cells, etc.)
- Advancements in ASIC technology are driving development cost for advanced ASICs
- Parametric modeling may provide a viable solution for micro-electronic development and production cost estimation

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ASIC Basics

- Application Specific Integrated Circuit
  - Custom designed for a specific application
  - Multilayered integrated circuit design
  - Hardwired to allow for high speed operation
  - Overall increased computational capacity over non-ASIC devices
- Varieties of ASICs
  - Full Custom
  - Standard Cell
  - Structured Cell
  - Gate Array
- ASIC Design Cost Drivers
  - Technology node
  - Die Size
  - Number of Gates (total gates vs. logic gates)
  - I/O Pinouts
  - Packaging

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The ASIC Solution

- ASIC Characteristics
  - Favorable Size, Weight and Power Characteristics
  - High speed operating capability
  - Overall increased computational capacity
- ASIC Applications
  - Commercial market has driven widespread use of ASIC devices in various applications (Wireless devices, PDAs, Gaming Platforms)
  - Military electronics have been adapting ASIC devices into their design applications to increase performance in challenging environments

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Micro-Electronic Development Cost Trends

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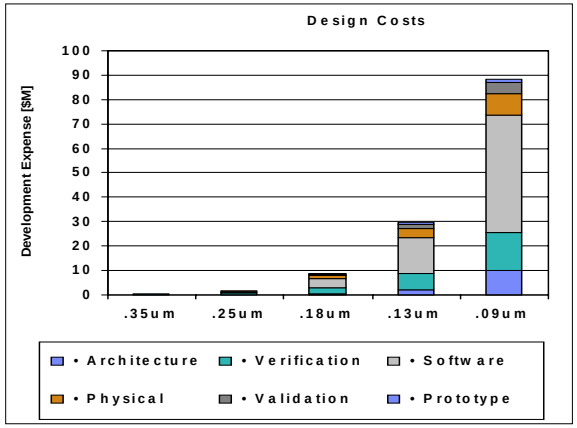
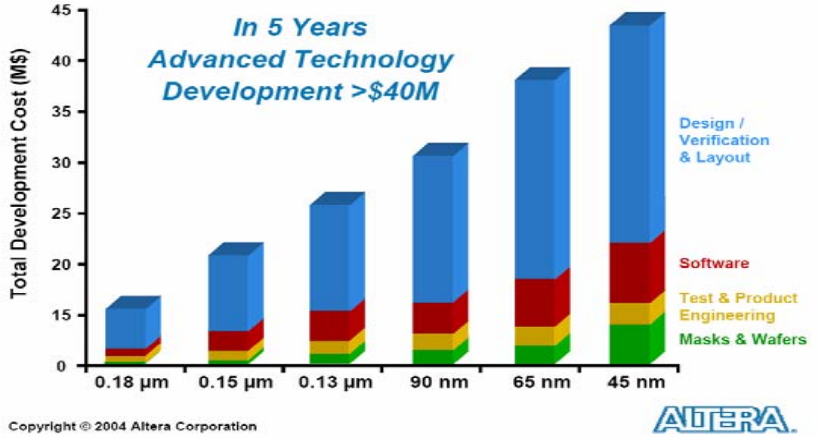
…But wait, there's more…Complexity and Cost



Source: IBS, Inc.

Increasing Development Cost



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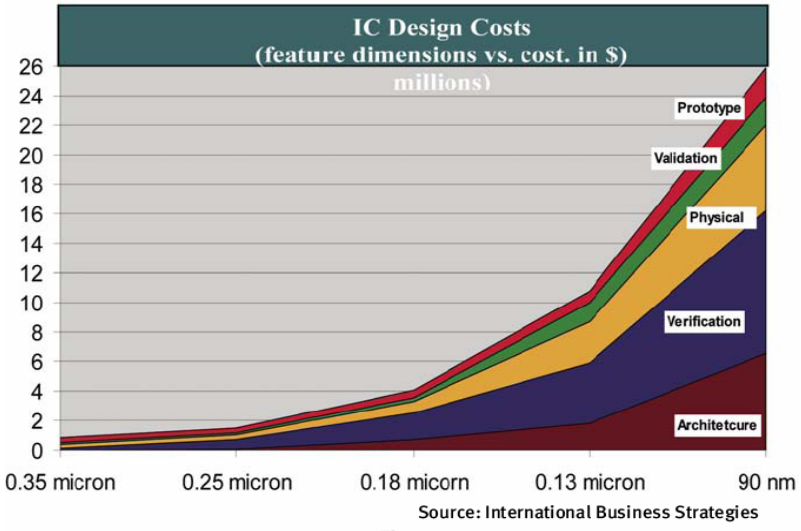

Source: International Business Strategies

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Our Estimating Challenge

- Estimating ASIC Devices by Analogy
  - Not applicable/conducive to CER development
  - Historical data not readily available
  - Detailed design knowledge necessary
  - Limited space applications
- Parametric Cost Modeling of ASIC Devices
  - Knowledge Bases provide a reasonable starting point when not all design parameters are known
  - Ability to customize knowledge bases
  - Ability to calibrate against existing knowledge bases
  - Establishes a framework for future improvements and updates

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Our Approach Using SEER-IC

- SEER-IC Cost Model Assessment
  - ASIC data request to MILSATCOM contractors
  - Extensive interviews with space vehicle contractors to collect the required ASIC technical parameters and associated cost data
  - Modeled 24 space ASIC devices in SEER-IC for comparison with actual development cost data
  - Reviewed both the quantitative technical parameters and qualititative assessment settings with contractors for the ASICs modeled
  - Emphasis on capturing the technical aspects of each ASIC device in SEER-IC model
  - Final Modeling Adjustments

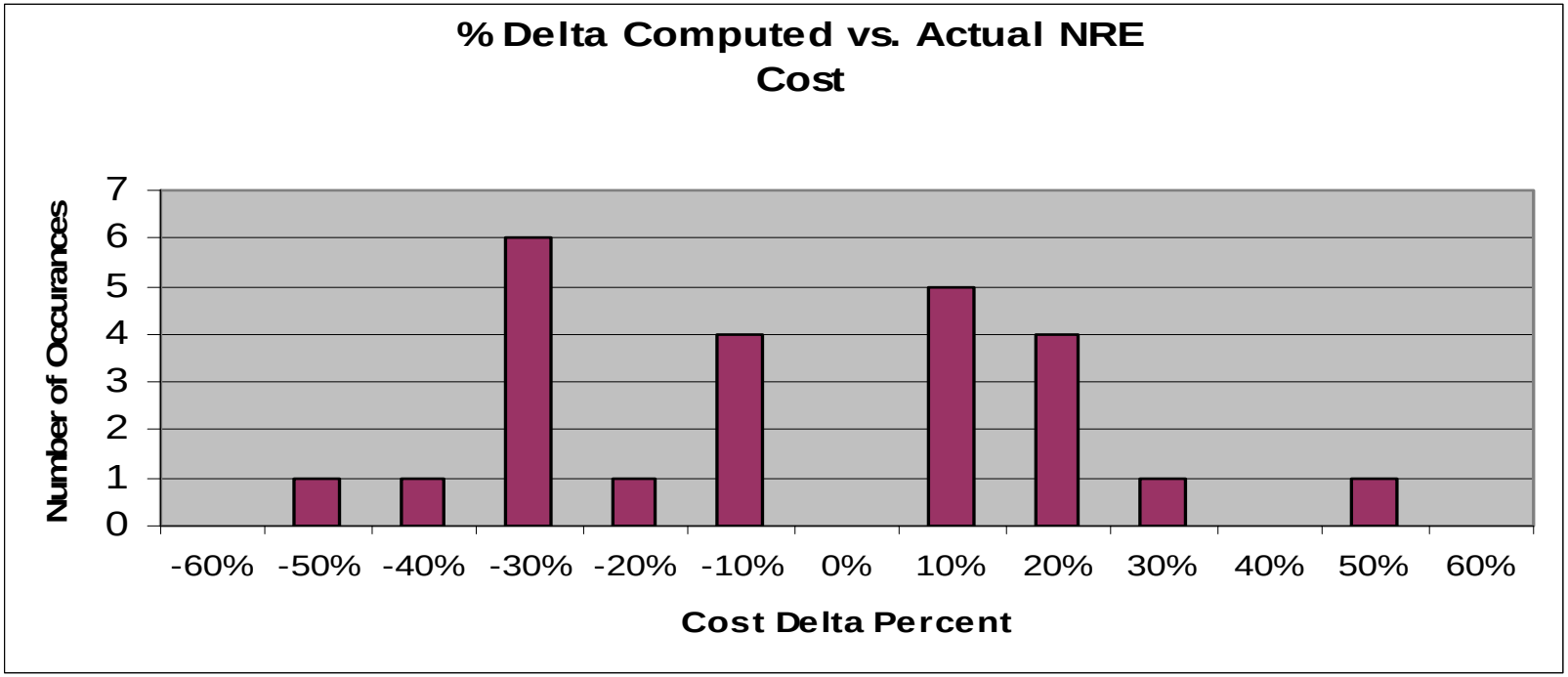
ASIC Modeling in SEER-IC

PRODUCT DESCRIPTION			
- Chip Area (sq mm)	100.00	100.00	100.00
- Feature Size (micron)	0.09	0.09	0.09
- Transistors Per Chip	0	0	0
- Gates Per Chip	1,000,000	2,000,000	3,000,000
- Input/Output Pins Per Chip	100	100	100
- Process Type		CMOS	
- Package Type		Ball Grid	
- Wafer Diameter (mm)	200.00	200.00	200.00
- Operating Frequency	Low	Low	Low
MISSION DESCRIPTION			
- Chip Classification		Custom	
- Operating Environment		Military	
PROGRAM DESCRIPTION			
- New Design	50.00%	50.00%	50.00%
- Iterations	1	1	1
- Certification Level	Nom+	Nom+	Nom+
DEVELOPMENT ENVIRONMENT			
- Developer Capability & Experience	Nom	Nom+	Hi-
- Development Tools & Practices	VHi-	VHi	VHi
- Requirements Volatility	Low	Low	Low+
PRODUCTION ENVIRONMENT			
- Production Experience	Nom	Nom+	Hi-
- Production Tools & Practices	Nom	Nom+	Hi-
PROGRAM SCHEDULE			
- Start Date for Development		1/01/04	
- Prototype Quantity		22	
- Start Date for Production		1/01/05	
- Optional Specified Yield		80.00%	
PRODUCTION			
- Prior Production Units	0	0	0
- Total Production Quantity		2,000	
- Percentage of Item Purchased		0.01%	
- Production Unit Purchase Cost		0.00	
PROBABILITY		50.00%	
ECONOMIC FACTORS			
- Development Cost Wraps/Fee		0.00%	
- Production Cost Wraps/Fee		0.00%	

Technical Quantitative Parameters

Qualitative Parameters

ASIC Cost Modeling Comparison



- Initial Comparison Between Modeled and Actual Cost
  - Individual errors on modeled ASIC devices were significant
  - Ensemble error on modeled ASICs were reasonable

Post SEER-IC Adjustments

- ASIC Cost Modeling Comparison
  - Reviewed outlier points to distinguish complexity
  - Error in cost data provided by contractors
  - Individual ASIC complexity is lost in grouped actual cost data provided by contractors
- Post SEER-IC Calibration Adjustments
  - Applied an adjustment factor to each of the individually modeled ASIC devices to minimize ensemble error
  - Adjustment factor is only applicable to these specific data, not one size fits all

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Summary

- ASIC technology is becoming more prevalent in Military electronics applications with standard cell ASICs leading the other ASIC types in popularity
- ASIC development costs are continuing to increase and need to be estimated separately from electronic board cost estimation
- Parametric cost modeling of ASIC devices provide a viable method of estimating the development cost of these devices provided research continues on advancements in the industry and the models are updated regularly

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Future Related Topics

- Advanced Technology Node Calibration Studies
  - Calibration of SEER-IC/H at advanced technology nodes
- Other Micro-Electronic Applications
  - Field Programmable Gate Arrays (FPGAs)
  - Multi-Chip Module (MCM) technologies
  - System On a Chip (SOC) technologies
- Model Comparison Between SEER-IC and SEER-H
  - Compare the enhanced modeling capability of SEER-H (IC module) with the previous SEER-IC model

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